a gate formed on the silicon carbide tub; and

source and drain regions located in the silicon carbide tub and laterally offset from the gate; and

a complimentary metal-oxide semiconductor (CMOS) device formed on the conductive substrate, the CMOS device having a tub comprising a material different from the silicon carbide tub.

45. (Previously Presented) The semiconductor device as recited in Claim 44 wherein the MOSFET has a breakdown voltage greater than an operating voltage of the CMOS device.

46. (Previously Presented) The semiconductor device as recited in Claim 44 wherein the MOSFET has a breakdown voltage of at least about 10 volts and the CMOS device has a breakdown voltage between about 3 volts and 5 volts.

47. (Previously Presented) The semiconductor device as recited in Claim 44 wherein the semiconductor device is a power converter and the MOSFET is a power switch for the power converter.

Claim 48 was previously canceled without prejudice or disclaimer.

49. (Previously Presented) The semiconductor device as recited in Claim 44 wherein the silicon carbide tub is located over the conductive substrate.

50. (Previously Presented) The semiconductor device as recited in Claim 44 wherein the material is doped silicon, wherein the silicon is doped with a p-type dopant or an n-type dopant.

51. (Previously Presented) The semiconductor device as recited in Claim 44 wherein the source and drain regions are doped with a p-type dopant or an n-type dopant.

52. (Previously Presented) The semiconductor device as recited in Claim 44 further comprising a buried oxide layer formed in the conductive substrate.

53. (Previously Presented) The semiconductor device as recited in Claim 44 wherein the conductive substrate comprises silicon and wherein the silicon carbide tub comprises a 3C silicon carbide.

54. (Previously Presented) A semiconductor device, comprising:

a lateral metal-oxide semiconductor field effect transistor (MOSFET), including:

a silicon carbide tub located within or contacting a conductive substrate;

a gate formed on the silicon carbide tub; and